The Role of a Compact Low Voltage FE-SEM in Semiconductor Failure Analysis

Application Note

Introduction

Progress of semiconductor devices has rapidly accelerated toward high integration, high density and high functionality. In addition, use applications are widely penetrated into various consumer and industrial fields.

Failure analysis is the process of investigating semiconductor devices after failure is observed by electric measurement, and by physical, microscopy and chemical analysis techniques necessary to confirm the reported failure and clarify the failure mechanism. It relies on collecting failed components for subsequent examination of the cause or causes of failure using a wide array of methods. The NDT (nondestructive testing) methods are valuable because the failed products are unaffected by analysis, so inspection usually starts using these methods. "Microelectronics Failure Analysis Desk Reference" 5th edition published by ASM International is a good reference which covers the plethora of techniques employed in semiconductor failure analysis.

Typical analysis includes but is not limited to the following:

- Image – Optical, Thermal imaging, FE-SEM (including EDS), AFM (including derivative modes, conductive AFM, electric force, Kelvin Probe AFM, Scanning Capacitance, Scanning Microwave Microscopy, etc.), and FE-AES images of device on wafer or depackaged
- Surface – FE-AES survey, x-y mapping, and depth/ composition profiles
- Chemical analysis – FT-IR microspectroscopy analysis, SEM based EDS analysis
- Structural – FE-SEM and TEM cross-sectioning, X-Ray imaging
- Electrical characterization – I/V curves and parametric analysis
- Relating visual images with operating function, or failure
- Relating chemical composition and electrical data with operating function or failure
- Relating internal structure, or failure, to the design, engineering, manufacturing, or operation

Of the multitude of scientific instrumentation used to characterize semiconductor device failures, SEM is one of the most common instruments. Because of the ubiquitous need for SEM images in failure analysis, a new breed of instruments, the compact or bench top SEM, is garnering attention. These smaller SEMs will not replace the full suite of analytical capabilities of the full-size instruments; however, their ease of use and quick, high resolution images allows operators with a wider range of SEM skill level. The compact SEM improves overall efficiency and analysis time; allowing researchers to quickly image the device when only an image is needed to guide further analysis thereby enabling the highly skilled operator of the full-sized SEM to focus on the more complicated analyses.

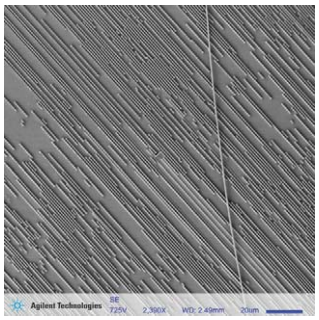

Figure 1. Deprocessed chip metal conductor lines.

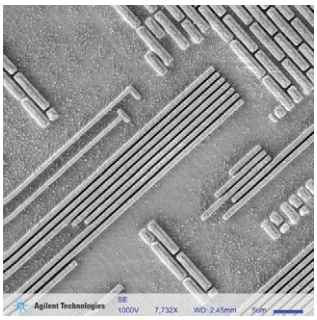

Figure 2. Deprocessed chip metal conductor lines.

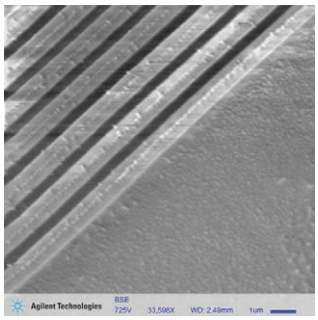

Figure 3. Deprocessed chip metal conductor lines.

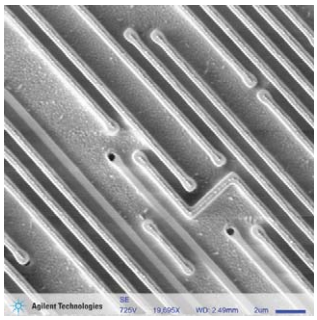

Figure 4. Deprocessed chip metal conductor lines.

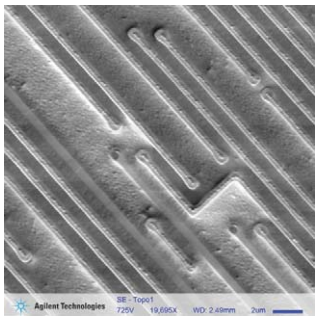

Figure 5. Deprocessed chip metal conductor lines, topographic shading image from Figure 4.

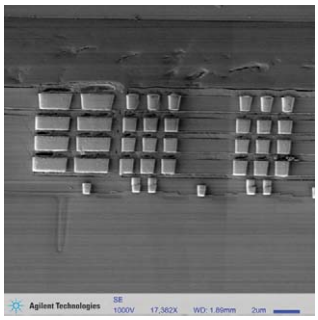

Figure 6. Etch defect resulting in non-through via.

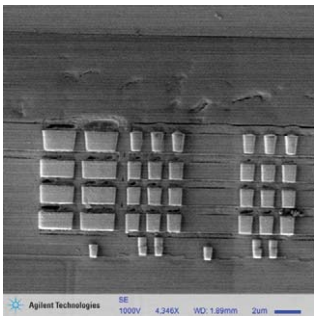

Figure 7. Etch defect resulting in non-through via.

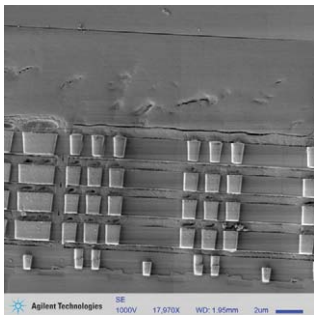

Figure 8. Etch defect resulting in non-through via.

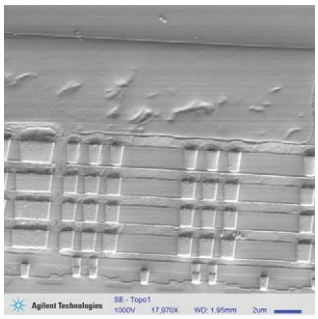

Figure 9. Etch defect resulting in non-through via, topographic shading image.

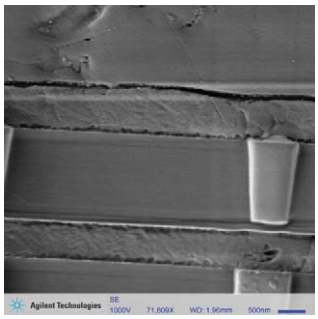

Figure 10. Etch defect resulting in non-through via.

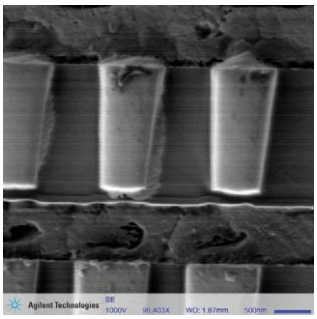

Figure 11. Etch defect resulting in non-through via.

Agilent's 8500 compact FE-SEM is a low voltage, field emission SEM which employs a novel electrostatic lens design. This innovative design allows for high resolution imaging of semiconductor devices, typically without the need for metal coating. The 8500 FE-SEM was used to image metal lines on a deprocessed chip package, Via defects, a 45nm gate structure, and a BGA contact pad.

Deprocessed Chip Metal Lines

After NDT analysis, typically the next step is deprocessing or unsealing the chip. The purpose of unsealing is to expose the surface of the chip without damaging the surface of the silicon chip, the wire and the lead frame and to make later observations and measurements. The device, with the surface of the chip exposed by deprocessing, is observed with a compact FE-SEM, see Figures 1–5. The state of chips, the state of die bonds, the state of wires and the state of leads are observed carefully. The abnormalities typically detected by internal observations are as follows: attachment of foreign materials, pattern abnormalities, wire breakage, short-circuits, corrosion of Al wires or traces, and cracks on passivation films.

Via Defects

To increase device bandwidth, reduce power and shrink form factor, microelectronics manufacturers are implementing three dimensional chip stacking using through silicon vias. Chip stacking with through silicon vias combines silicon and packaging technologies. As a result, these new structures have unique manufacturing and reliability requirements.

Via formation is typically accomplished by etching using a deep reactive ion etching process. However, if this etch fails to sufficiently "drill through" the metal via will not make electrical contact to the layer below. Figures 6–11.

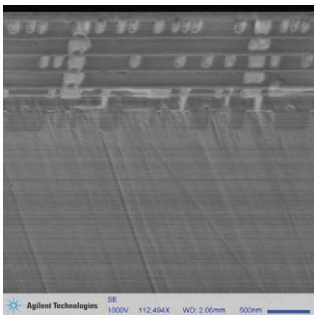

Figure 12. 45 nm node gate stack.

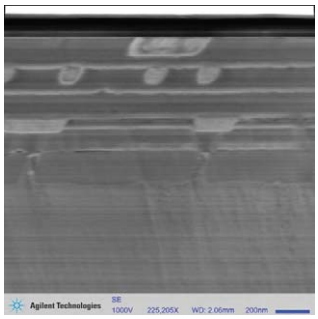

Figure 13. 45 nm node gate stack.

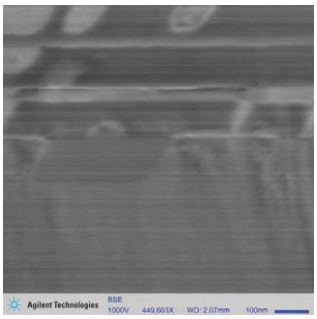

Figure 14. 45 nm node gate stack.

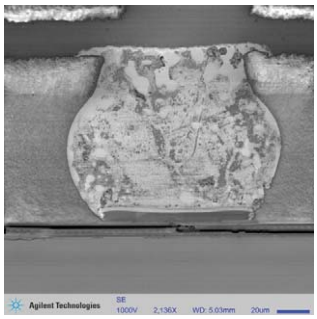

Figure 15. BGA contact pad.

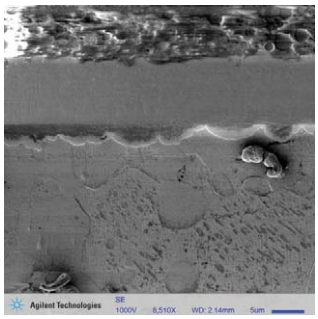

Figure 16. BGA contact pad, board contact interface.

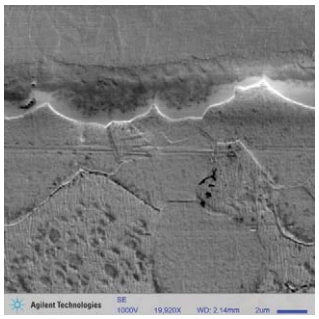

Figure 17. BGA contact pad, board contact interface.

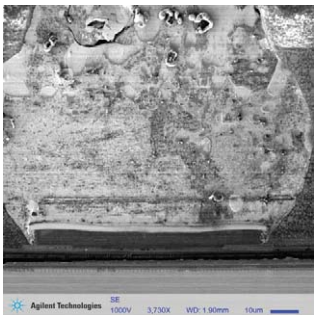

Figure 18. BGA contact pad, IC chip contact interface.

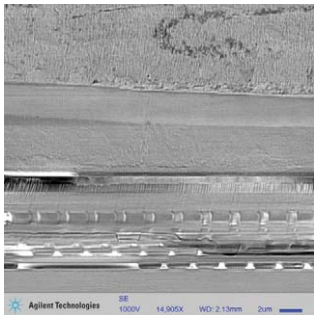

Figure 19. BGA contact pad, IC chip contact interface.

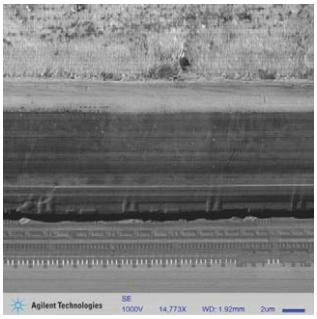

Figure 20. BGA contact pad, IC chip contact interface.

45 nm Gate Structure

One of the key methods to enable transistor gate length scaling over the past several generations has been to scale the gate oxide. This improves the control of the gate electrode over the channel, enabling both shorter channel lengths and higher performance. As the gate oxide was scaled the gate leakage current increased and the scaling of the gate oxide slowed as a result of the power limitations from the increased gate leakage. In order to overcome these limitations at the 45 nm structures, new high dielectric constant materials had to be developed. With the decreasing scale challenges arise in imaging the structures for both geometry and material composition. Previously visualizing 45 nm gate structures has been unattainable with compact SEM instruments. However, with the advent of the compact FE-SEM, these structures can now be imaged for the first time. Figures 12–14.

BGA Contact Pad

Failure analysis of BGA (ball grid array) devices can be daunting. The primary advantage of BGA packaging is the packing of large numbers, upwards of 500, of input-output pins into a relatively small area. The high number of connections is also what makes the failure analysis task so complex. Two of the most common failure modes are black pad syndrome and die cracking. Black pad syndrome is related to residual phosphorus from electroless metal plating, causing a weak layer during solder reflow. Die cracking is related to thermal expansion mismatch of materials or mechanical flexing of the printed circuit assembly.

SEM examination of a BGA cross section was performed to look for both of these failure modes, see Figures 15–20. Upon close inspection of the solder interface, Figures 16–18, no evidence of black pad syndrome was observed. However in Figures 19 and 20, evidence of die cracking is visible within the IC device.

Conclusions

Low voltage compact FE-SEM provides ease of use and a straightforward technique for high resolution imaging of semiconductor device structures, typically without the need for metal coating to dissipate charge buildup. Although the application range of the semiconductor samples examined spans many levels of sophistication in materials, design, and processing, the morphological features of interest and defects could easily be investigated with the Agilent 8500 FE-SEM.

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